REMARKS

Applicant thanks Examiner for the detailed review of the application.

Claim Rejections -35 USC § 103(a)

The Office Action has rejected Claims under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,195,728 to Bordaz et al. (referred to hereinafter as "Bordaz") in view of US. 6,134,631 to Jennings et al. (herein referred to as "Jennings").

"The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144). The Office Action has failed to meet one or more of these requirements.

The office action states that Bordaz includes cache memories 5, 15, 45, and 65 that comprise remote caches which may hold local and remote data. However, caches 5, 15, 45, and 65 are **included within** modules 5, 25, 45, and 65. As can be seen from applicant's Figure 1, as separate shared cache is coupled **separately** from the other processor cores (i.e. P0, P2, and P6 each include a private cache, while shared cache **10**, which is separate and coupled separately from P0, P2, and P6 in ring **15**. Therefore, Bordaz does not teach of coupling processor cores to a separate cache in a ring configuration, but rather only coupling of modules in a ring, where **included within** each module is a remote cache. In other words, no remote cache is disclosed separate and coupled in ring 16 of Bordaz.

In contrast to Bordaz, applicant's claim includes "a share cache separate from the plurality of cores…a ring to connect the one or more processor cores and the shared cache." Similarly, claim 14 includes "a plurality of cores and a shared memory connected in a ring, the shared cache being separate from the plurality of cores." Claim 18 includes "a plurality of cores and a shared memory separately coupled with an unbuffered bi-directional ring interconnect." As stated above, Bordaz does not disclose a shared cache coupled separately in the ring or a cache separate from cores, as in applicant's claims. Furthermore, Jennings does not disclose coupling of cores and a shared cache in a ring. As a result, applicant respectfully requests that claims 1-20 are now in condition for allowance.

If there are any additional charges, please charge Deposit Account No. 50-0221. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact David P. McAbee at (503) 712-4988.

Respectfully submitted,
Intel Corporation

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